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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/026,371	12/24/2001	Kun-Yung K. Chang	R1-P102	8036

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DENIRO/RAMBUS
685 MARKET STREET, SUITE 540
SAN FRANCISCO, CA 94105

EXAMINER	
WONG, LINDA	

ART UNIT	PAPER NUMBER
2634	

DATE MAILED: 01/25/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/026,371	CHANG ET AL.	
	Examiner	Art Unit	
	Linda Wong	2634	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 November 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-41* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *27-30 and 39-41* is/are allowed.

6)☐ Claim(s) *1,7-10,14-16,18,20,22-24,31-32,36* is/are rejected.

7)☐ Claim(s) *2-6,11-13,17,19,21,25,26,33-35,37 and 38* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *14 November 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Response to Arguments

1. Applicant's arguments, see Applicant's Arguments, filed 11/14/2005, with respect to the rejection(s) of claim(s) 1-41 under Lee et al and have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of Trodden (US Patent No.: 5969576) in view of the admitted prior art (Figure 1).

Drawings

2. The drawings were received on 11/14/2005. These drawings are accepted.

Claim Rejections - 35 USC § 102

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. **Claims 1,7-9,14-15,20,22-24** are rejected under 35 U.S.C. 102(b) as being anticipated by Yoshizaki (US Patent No.: 6868134).

   a. **Claim 1**, Yoshizaki discloses a sampling unit (Fig. 3a, label 40), a select circuit (Fig. 3a, label 40 and 60) coupled to the sampling unit (Fig. 3a, labels 40 and 60), according to a clock or data rate select signal (Fig. 3, labels C0-C3), one of the plurality of samples to be a first selected sample of the input signal (Fig. 3a, label 61) and another of the plurality of samples to be a second selected sample of the input signal (Fig.3a, label 62) and a phase control circuit coupled to receive the first and second selected samples of the input signal (Fig. 3a,

label 70) and to compare the first selected sample with the second selected sample to determine a relative position of the first clock signal (Col. 1, lines 45-59, Col. 2, lines 38-41 and lines 49-55), wherein the relative position of the first clock signal is selected from one of the first clock signal leads a transition of the input signal and the first clock signal lags the transition of the input signal. (Col. 6, lines 43-49, lines 54-61)

b. **Claim 7,** Yoshizaki discloses the first clock signal comprises a plurality of component clock signals each being offset in phase from one another. (Fig. 3a, labels C0,C1,C2 and C3 and Col. 4, lines 45-49)

c. **Claim 8**, Yoshizaki discloses the first clock comprises component clock signals having a phase angle such that transitions of the component clock signals occur at evenly spaced intervals with a cycle of a first one of the component clock signals. (Col. 4, lines 45-56)

d. **Claim 9,** Yoshizaki discloses the first clock has M component clock signals (Fig. 3a, labels C0,C1,C2 and C3), wherein each one of the component clocks captures a sample of the input signal during each cycle. (Col. 4, lines 45-49)

e. **Claims 14 and 15** inherit all the limitations of claim 1.

f. **Claim 18** inherits all the limitations of claim 1.

g. **Claim 20**, Yoshizaki discloses choosing another sample with a different phase based on the comparison from the phase decoder. (Fig. 3A, labels 70,80 and 61-64, Abstract, lines 23-31, Col. 6, lines 54-61)

h. **Claim 22**, Yoshizaki discloses determining the phase difference, which would inherently detect a transition between the two sample data.

i. **Claims 23 and 24**, Yoshizaki discloses a sampling an input signal with a plurality of phase offset clock signals. (Fig. 3A, labels sin,C0,C1,C2 and C3)

4. **Claims 10 and 21** are rejected under 35 U.S.C. 103(a) as being unpatentable over Yoshizaki (US Patent No.: 6868134).

a. **Claim 10**, Yoshizaki discloses a sampling unit comprising latches. (Fig. 3a, labels 47-59) The latches are each clocked by C0,C1,C2, and C3 respectively to shift the input data signal by each phase within the C0,C1,C2, and C3. (Fig. 3A, labels 47-59, C0,C1,C2 and C3, Col. 4, lines 56-68 and Col. 5, lines 1-26) It is well known in the art that latches act as temporary storage units. Although Yoshizaki does not disclose using a shift register, it would be obvious to one skilled in the art to replace the latches with shift registers due to inventor's design choice.

b. **Claim 21**, Although Yoshizaki fails to disclose detecting the value of the two comparing data samples, Yoshizaki discloses detecting the phase difference, which would inherently disclose determining the values since detecting the phase difference would also determine the magnitude of the samples.

5. **Claims 16,31-32,36** are rejected under 35 U.S.C. 103(a) as being unpatentable over the admitted prior art (Fig. 1 and pages 2-4) in view of Yoshizaki (US Patent No.: 6868134).

   a. **Claim 16**, the admitted prior art discloses a phase mixer to interpolate between a selected one of the phase vectors (Fig. 1, label 103) to generate the first clock signal, the phase mixer to receive the phase control signal from the phase control circuit and to adjust the phase according to the phase control signal. (Fig. 1, labels 111 and 113 and page 2, paragraph [0004]) It would be obvious to one skilled in the art to incorporate Yoshizaki's invention into the admitted prior art to provide fast synchronization of the incoming data signal and minimize the loss of incoming data.

   b. **Claim 31**, the admitted prior art discloses an output driver. Although the admitted prior art does not disclose a serializing circuit and a select circuit, Yoshizaki discloses a serializing circuit to receive a first parallel set of bits (Fig. 3a, label sin) and to output a set of bits in sequence (Fig. 3a, outputs from label 40) and a select circuit coupled to the serializing circuit to select (Fig. 3a, labels 60 and 40), according to a data rate select signal (Fig. 3a, labels c0,c1,c2 and c3), data bits within the outbound data value to form a first parallel set of bits received within the serializing circuit (Fig. 3a, labels 40, and 60). It would be obvious to one skilled in the art to incorporate the sampling unit and multiplexor as disclosed by Yoshizaki into the admitted prior art's invention to provide fast

synchronization of the incoming data signal and minimize the loss of incoming data.

c. **Claim 32**, Yoshizaki discloses two clocks sampling rates with different phases (Col. 4, lines 45-49), wherein the clocks samples the input data signal (Fig. 3a, label sin) output a first parallel set of bits and a second parallel set of bits. (Fig. 3a, outputs from label 40) The selectors (fig. 3a, label 60) selects from the first and second parallel set of bits, respectively, a first portion of the outbound data value and a second portion of the outbound data value. (Fig. 3a, outputs from label 40 to label 60 and output from labels 61-64)

d. **Claim 33**, Yoshizaki discloses a variable sampling rate or clocks, which inherently indicates that, depending on the sampling rate, the a pair of samples will be selected or a signal sample is selected.

e. **Claim 34**, Yoshizaki discloses multiple sampling rates or clocks and a selecting circuit. Although Yoshizaki does not discloses the selection circuit is adapted to select the entire outbound data value to form the received first parallel set of bits, Yoshizaki inherently discloses selecting a data value or a outbound data value using a second clock. (Fig. 3a, label 62)

f. **Claim 35**, Yoshizaki discloses multiple data rates or data clocks for sampling the input signal. (Fig. 3a, label c0-c3) It would be obvious to one skilled in the art, based on designer choice, to have a single data rate and/or a double data rate.

g. **Claim 36** inherits all the limitations of claim 31.

6. **Claims 11-13, 25-30 and 39-41** are rejected under 35 U.S.C. 103(a) as being unpatentable over Sacks et al (US Patent No.: 6181505) in view of Yoshizaki (US Patent No.: 6868134).

   a. **Claims 11 and 13** inherit all the limitations of claims 25 and 26.

   b. **Claim 12**, Although Yoshizaki does not disclose register for storing a sampling data rate, Sacks et al discloses an output to output the data rate select signal to the select circuit. (Fig. 2, labels 144, 258 and 250) It would be obvious to one skilled in the art to replace the clock sampling rates as disclosed by Yoshizaki with the data sampling rate stored in a register as disclosed by Sacks et al to provide the optimum variable sampling rate so to eliminate aliasing.

   c. **Claims 25 and 26**, Although Yoshizaki does not disclose a register for storing a variable sampling rate, Sacks et al discloses a register for storing a sampling rate and receiving the value from an external device. (Fig. 2, label 144,258) It would be obvious to one skilled in the art to replace the clock sampling rates as disclosed by Yoshizaki with the data sampling rate stored in a register as disclosed by Sacks et al to provide the optimum variable sampling rate so to eliminate aliasing.

   d. **Claim 27**, Yoshizaki discloses a sampling unit within a clock recovery unit (Fig. 3a, label 40 and Abstract, line 1). Although Yoshizaki fails to teach a register for storing a variable sampling rate value, Sacks et al disclose outputting a value indicative of a data rate to the integrated circuit device (Fig. 2, labels 144

and 150) and outputting a command (Col. 5, lines 20-30) to store the value in a configuration storage circuit within the integrated circuit device (Fig. 2, labels 144 and 258), the configuration storage circuit coupled to a PLL circuit within the integrated circuit device used for recovering a clock signal from the input signal. (Fig. 2, labels 276,258,272,254,256,250 and Col. 6, lines 3-26) It would be obvious to one skilled in the art to replace the clock sampling rates as disclosed by Yoshizaki with the data sampling rate stored in a register as disclosed by Sacks et al to provide the optimum variable sampling rate so to eliminate aliasing.

e. **Claim 28**, Sacks et al discloses the sampling rate is dependent on the type of data encoding and decoding schemes, thus, Sacks et al inherently discloses the sampling rate value is consistent with the operand data. (Col. 6, lines 30-33)

f. **Claim 29**, Sacks et al discloses the sampling rate would regulate the sampling of the input signal, which inherently discloses the value of the data rate is an operation code. (Col. 5, lines 20-30, Col. 6, lines 3-26)

g. **Claim 30**, Sacks et al inherently discloses the value of the number of data values with the input signal per a cycle of clock signal since the sampling rate has a metric unit of bits or bytes/second or a cycle.

h. **Claim 39** inherits all the limitations of claim 27, but claim 27 does not recite a selection unit. Yoshizaki discloses a selecting unit for selecting a first and second data sample from a first and second bound, respectively, wherein the

first and second sampled data are sampled by two different clocks. (Fig. 3a, labels 61,62,c0,c1,c2,c3 and 40) It would be obvious to one skilled in the art to incorporate the register storing variable sampling rates as disclosed by Sacks et al into Yoshizaki's invention to provide optimum sampling rates dependent on the data and prevent aliasing.

i. **Claim 40** inherits all the limitations of claim 28.

j. **Claim 41** inherits all the limitations of claim 29.

Allowable Subject Matter

7. **Claims 2-6,17,19,37-38** are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Linda Wong whose telephone number is 571-272-6044. The examiner can normally be reached on 9-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chieh Fan can be reached on (571) 272-3042. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Linda Wong

DACHA
PRIMARY EXAMINER